FIG.1

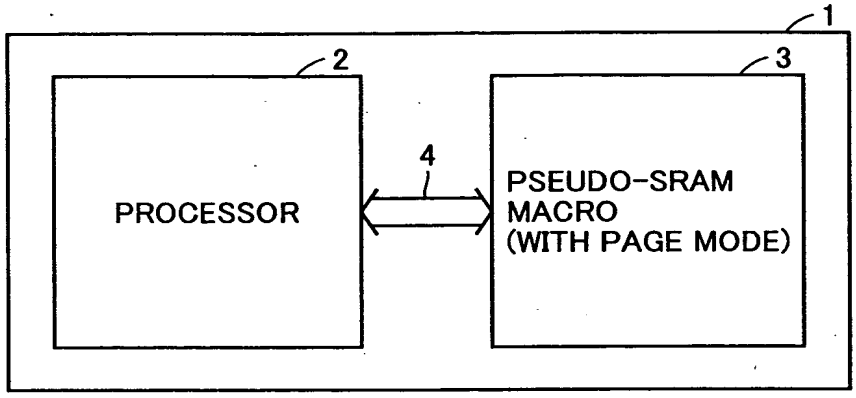

1
2
3
4
PROCESSOR
PSEUDO-SRAM
MACRO
(WITH PAGE MODE)

FIG.2

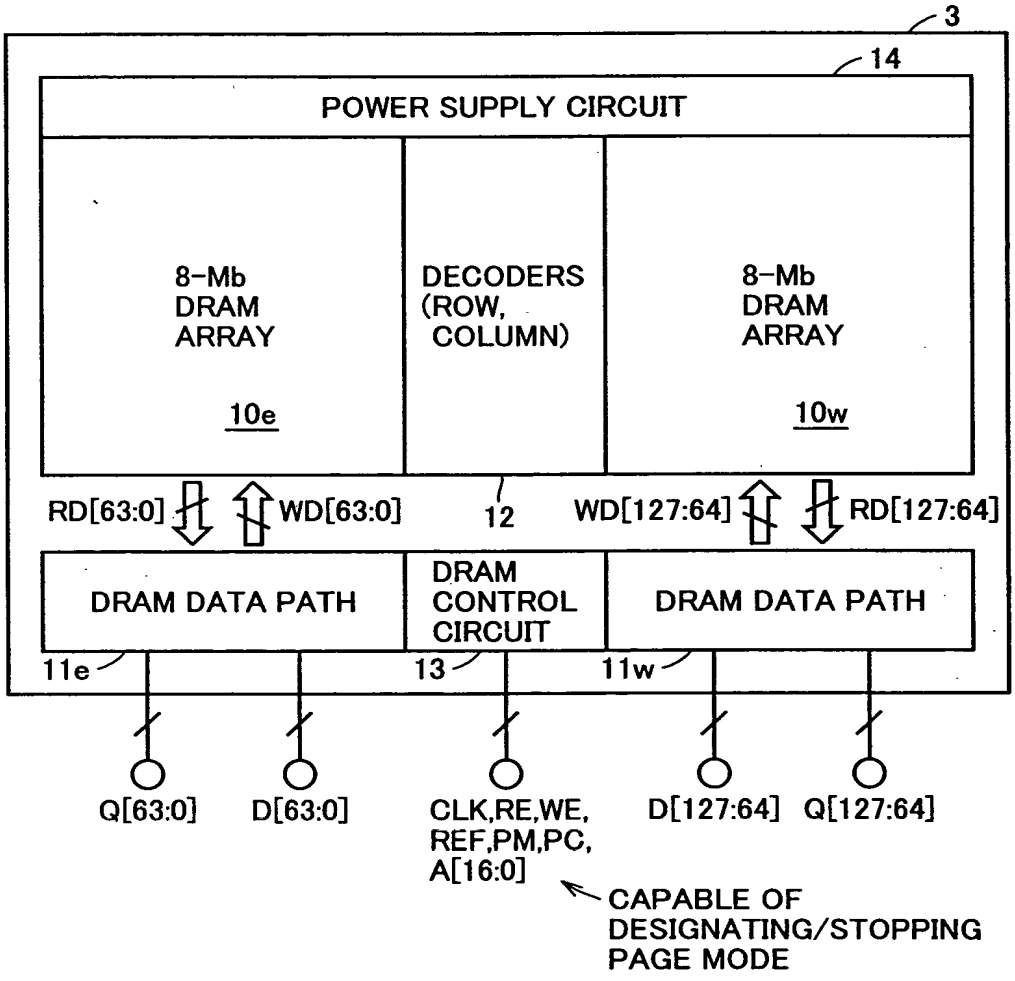

3
14
POWER SUPPLY CIRCUIT
8-Mb
DRAM
ARRAY
10e
DECODERS
(ROW,
COLUMN)
8-Mb
DRAM
ARRAY
10w
RD[63:0]
WD[63:0]
12
WD[127:64]
RD[127:64]
DRAM DATA PATH
DRAM
CONTROL
CIRCUIT
DRAM DATA PATH
11e
13
11w
Q[63:0]
D[63:0]
CLK,RE,WE,
REF,PM,PC,
A[16:0]
D[127:64]
Q[127:64]
CAPABLE OF
DESIGNATING/STOPPING
PAGE MODE

FIG.3

	CONTROL SIGNAL					FUNCTION
MNEMONIC	RE	WE	REF	PM	PC	
NOP	L	L	L	L	L	NO OPERATION
RE	H	L	L	L	L	READ, THEN CLOSE PAGE
REPM	H	L	L	H	L	READ, THEN KEEP PAGE OPEN
REPC	H	L	L	L	H	READ WHILE PAGE IS OPEN, THEN CLOSE PAGE
WE	L	H	L	L	L	WRITE, THEN CLOSE PAGE
WEPM	L	H	L	H	L	WRITE, THEN KEEP PAGE OPEN
WEPC	L	H	L	L	H	WRITE WHILE PAGE IS OPEN,THEN CLOSE PAGE
PC	L	L	L	L	H	CLOSE OPEN PAGE
REF	L	L	H	L	L	AUTO-REFRESH

FIG.4

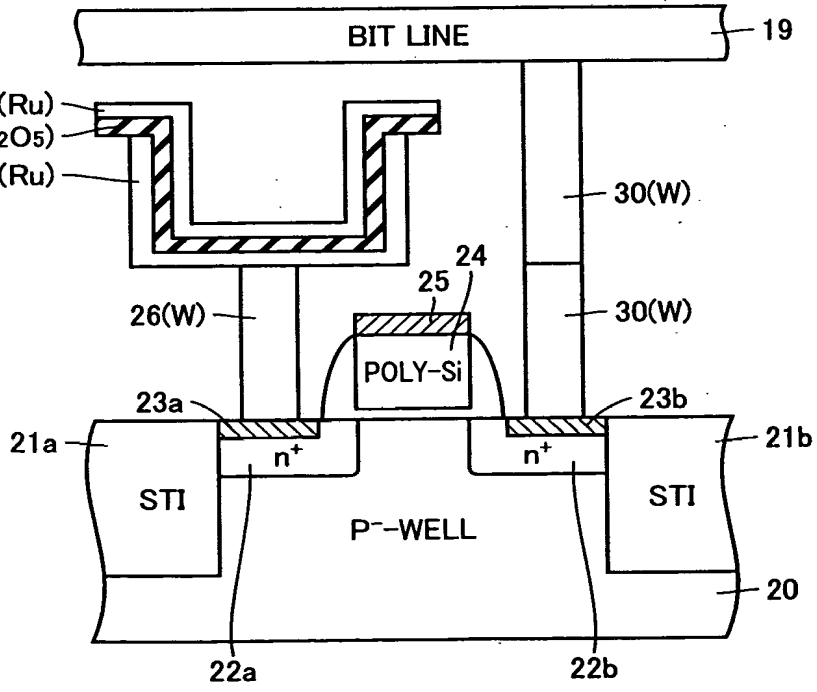


FIG.5

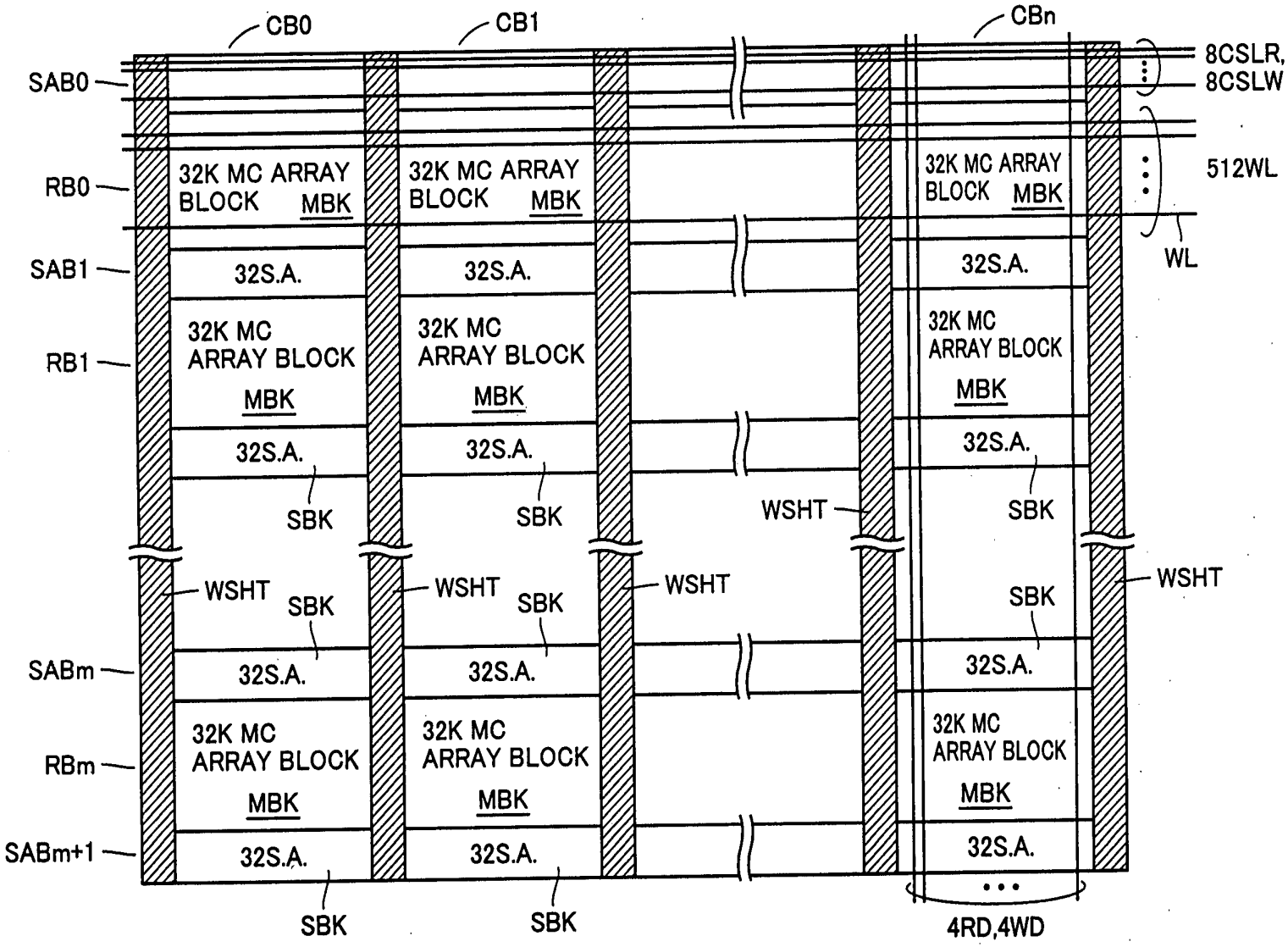

CB0
CB1
CBn
SAB0
RB0
SAB1
RB1
SABm
RBm
SABm+1
8CSLR,
8CSLW
512WL
WL
32K MC ARRAY BLOCK MBK
32S.A.
32K MC ARRAY BLOCK
MBK
SBK
WSHT
4RD,4WD

FIG.6

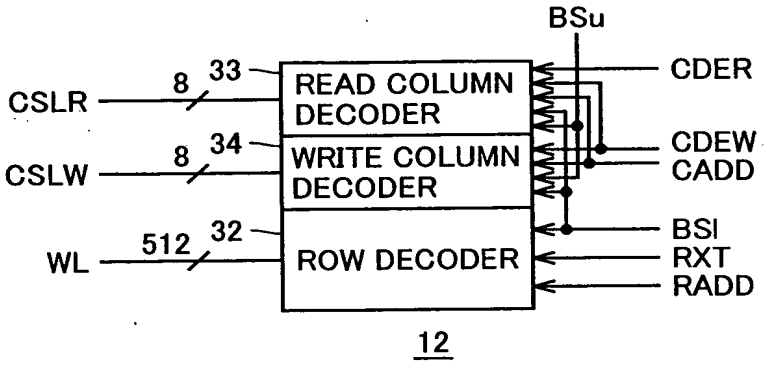

BSu
CSLR
8
33
READ COLUMN DECODER
CDER
CSLW
8
34
WRITE COLUMN DECODER
CDEW
CADD
WL
512
32
ROW DECODER
BSI
RXT
RADD
12

FIG.7

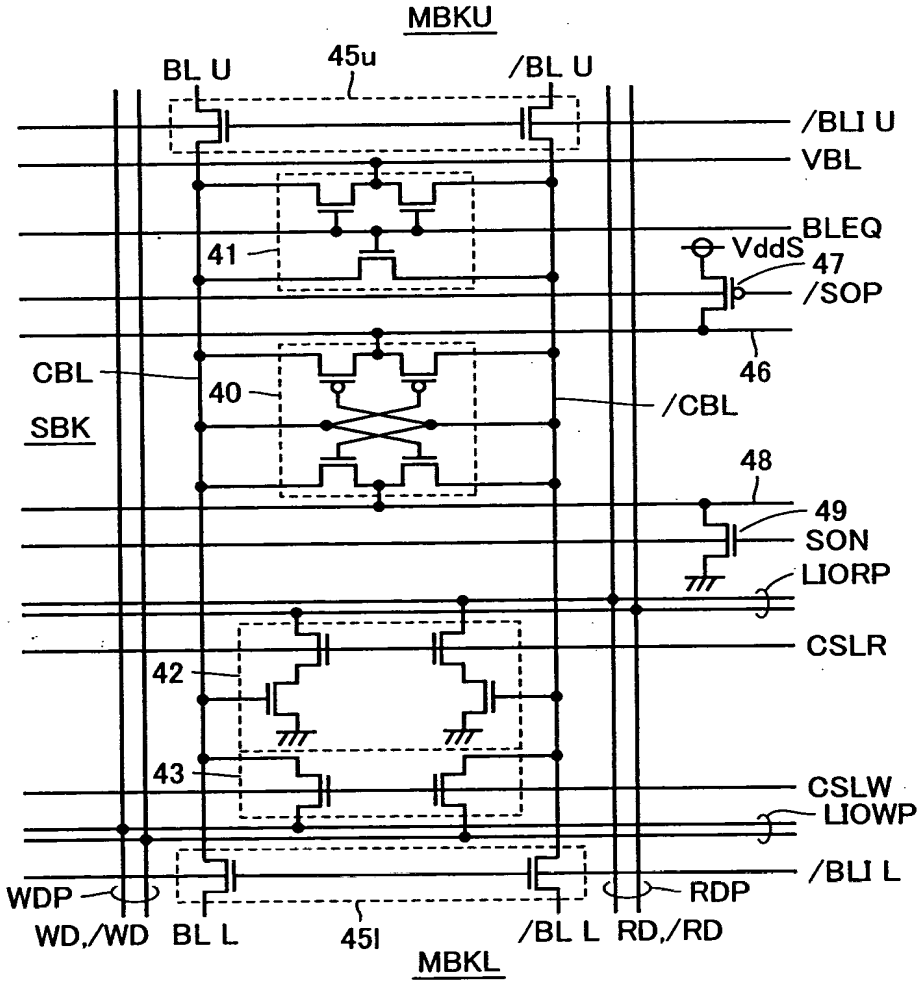

MBKU
BL U
45u
/BL U
/BLI U
VBL
BLEQ
VddS
47
/SOP
41
46
CBL
40
/CBL
SBK
48
49
SON
LIORP
CSLR
42
43
CSLW
LIOWP
/BLI L
WDP
RDP
WD,/WD
BL L
45l
/BL L
RD,/RD
MBKL

FIG.8

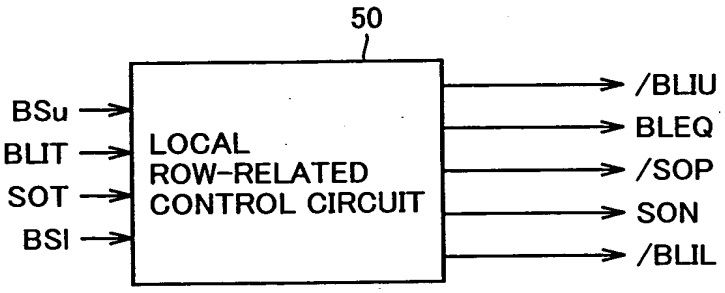

50
BSu
BLIT
SOT
BSI
LOCAL
ROW-RELATED
CONTROL CIRCUIT
/BLIU
BLEQ
/SOP
SON
/BLIL

FIG.9

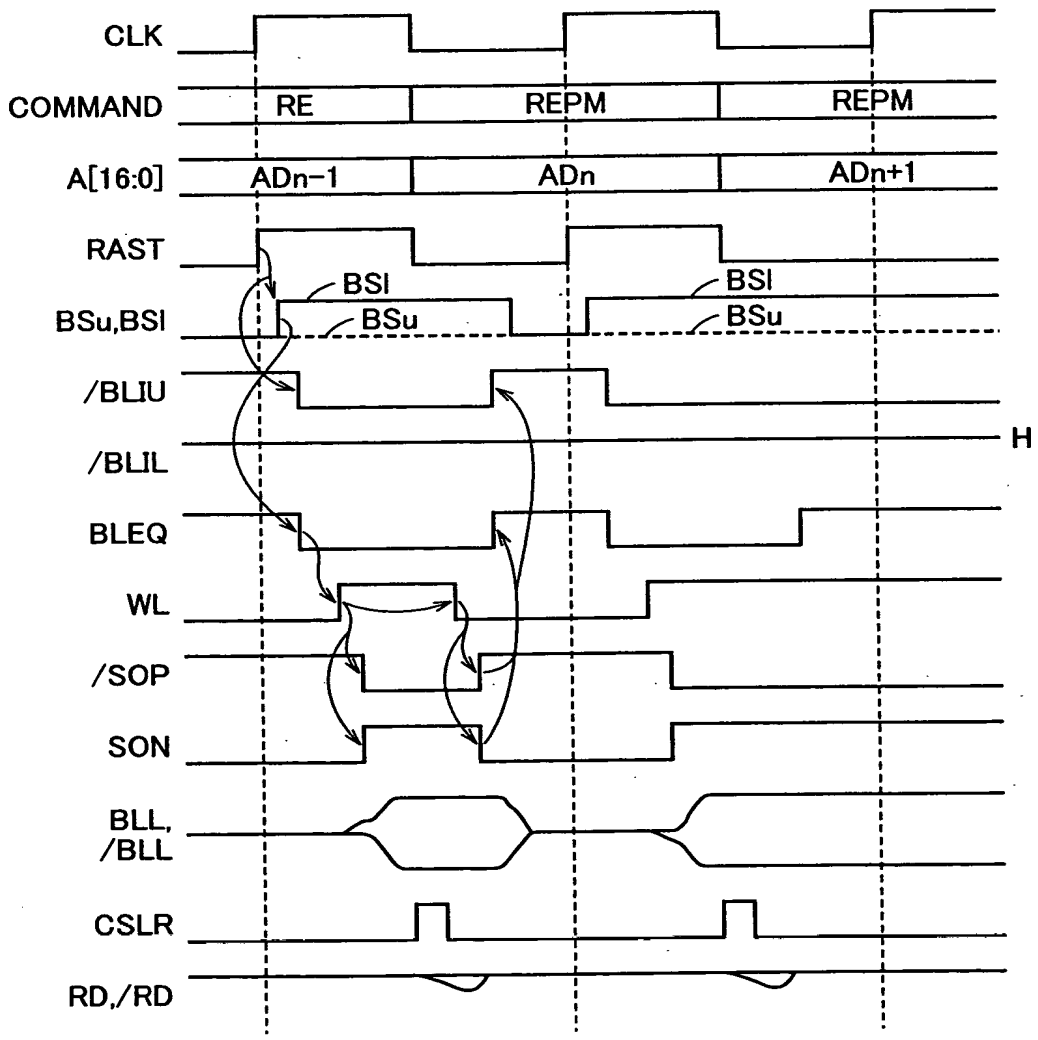

CLK
COMMAND
RE
REPM
REPM
A[16:0]
ADn-1
ADn
ADn+1
RAST
BSI
BSu
BSI
BSu
BSu,BSI
/BLIU
H
/BLIL
BLEQ
WL
/SOP
SON
BLL,
/BLL
CSLR
RD,/RD

FIG.10

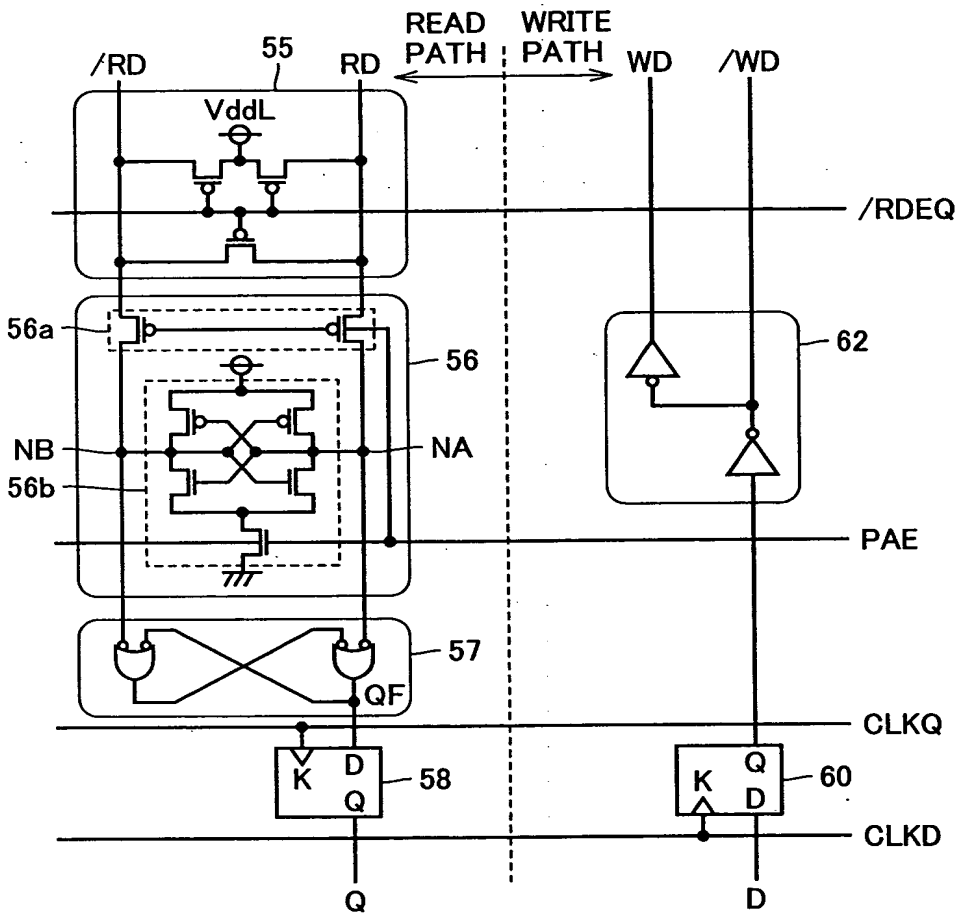

READ PATH
WRITE PATH
/RD
55
RD
WD
/WD
VddL
/RDEQ
56a
56
62
NB
NA
56b
PAE
57
QF
CLKQ
K
D
Q
58
K
Q
D
60
CLKD
Q
D

FIG.11

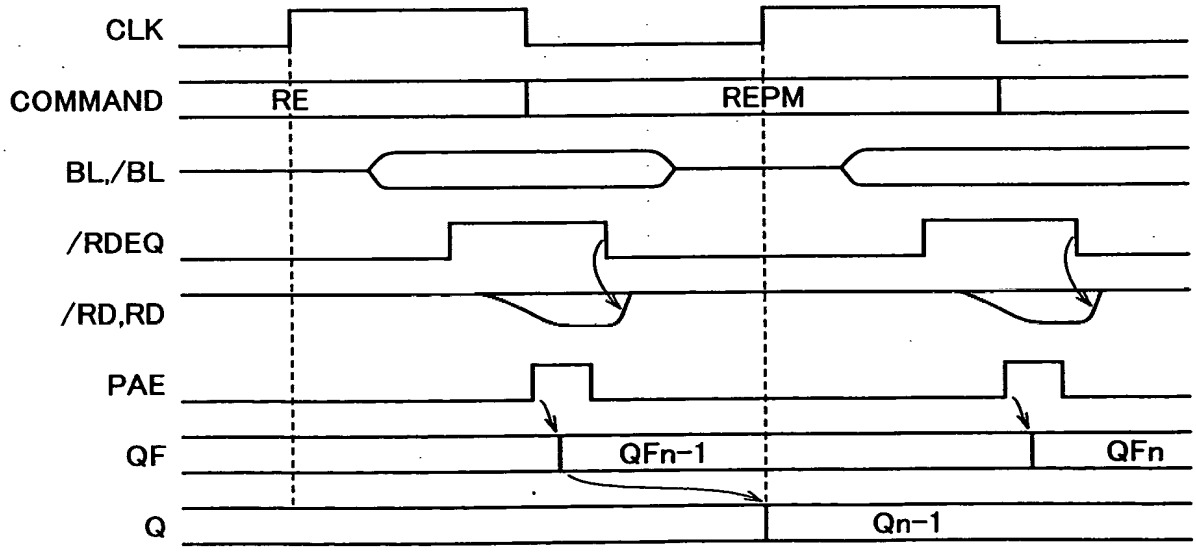

CLK
COMMAND
RE
REPM
BL,/BL
/RDEQ
/RD,RD
PAE
QF
QFn-1
QFn
Q
Qn-1

FIG.12

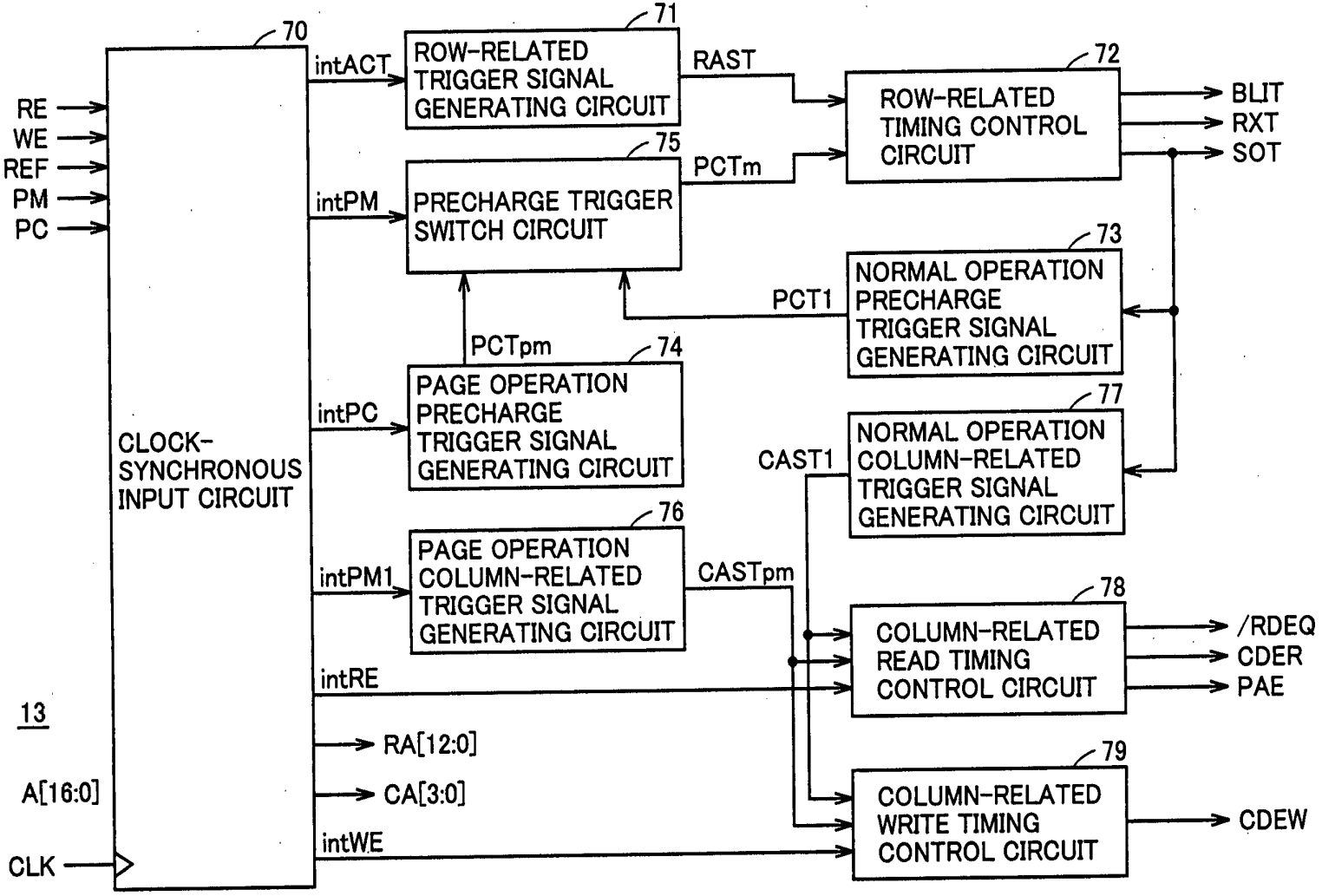

70
71
ROW-RELATED TRIGGER SIGNAL GENERATING CIRCUIT
intACT
RAST
72
ROW-RELATED TIMING CONTROL CIRCUIT
BLIT
RXT
SOT
RE
WE
REF
PM
PC
75
PRECHARGE TRIGGER SWITCH CIRCUIT
intPM
PCTm
73
NORMAL OPERATION PRECHARGE TRIGGER SIGNAL GENERATING CIRCUIT
PCT1
PCTpm
74
PAGE OPERATION PRECHARGE TRIGGER SIGNAL GENERATING CIRCUIT
intPC
77
NORMAL OPERATION COLUMN-RELATED TRIGGER SIGNAL GENERATING CIRCUIT
CAST1
CLOCK-SYNCHRONOUS INPUT CIRCUIT
76
PAGE OPERATION COLUMN-RELATED TRIGGER SIGNAL GENERATING CIRCUIT
intPM1
CASTpm
78
COLUMN-RELATED READ TIMING CONTROL CIRCUIT
/RDEQ
CDER
PAE
intRE
13
RA[12:0]
A[16:0]
CA[3:0]
79
COLUMN-RELATED WRITE TIMING CONTROL CIRCUIT
CDEW
intWE
CLK

FIG.13

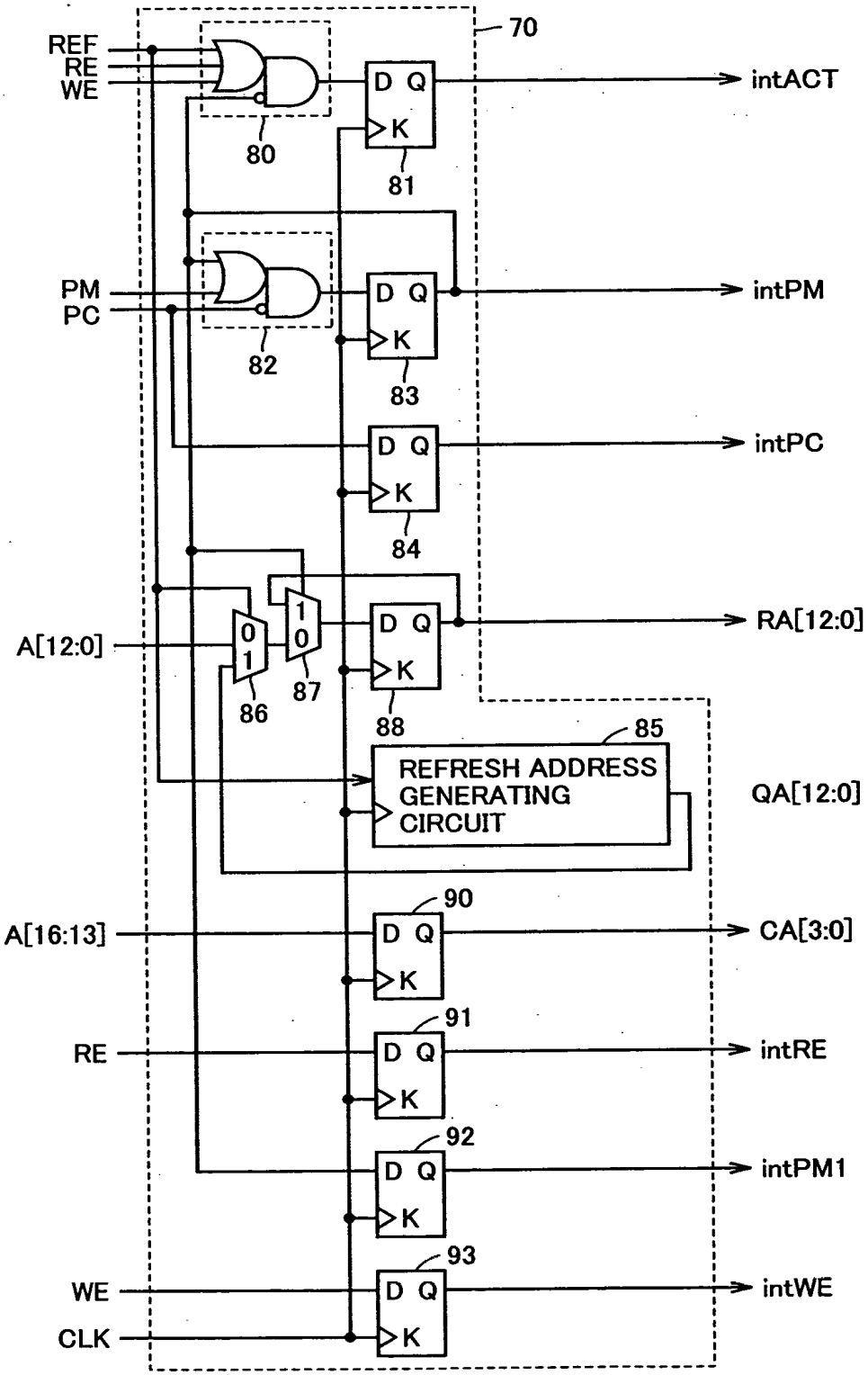

70
REF
RE
WE
80
D Q
K
81
intACT
PM
PC
82
83
intPM
intPC
84
A[12:0]
0
1
86
1
0
87
88
RA[12:0]
85
REFRESH ADDRESS GENERATING CIRCUIT
QA[12:0]
A[16:13]
90
CA[3:0]
RE
91
intRE
92
intPM1
WE
CLK
93
intWE

FIG.14

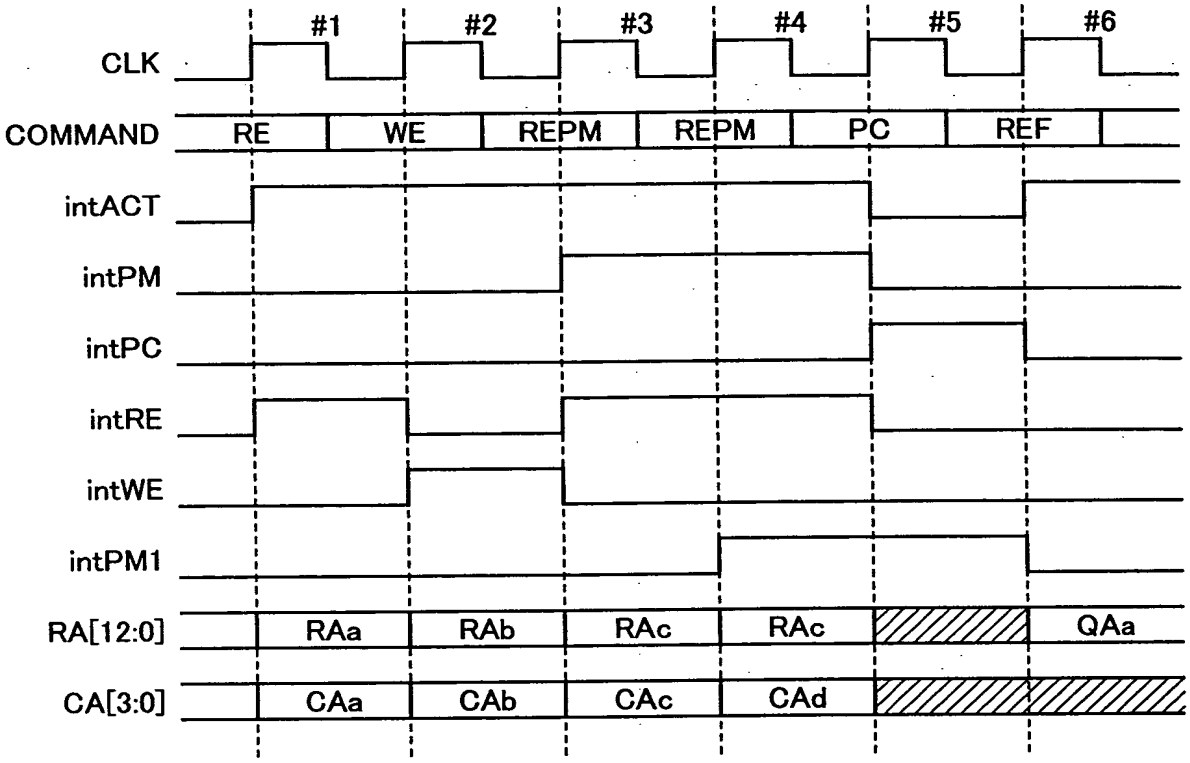

#1
#2
#3
#4
#5
#6
CLK
COMMAND
RE
WE
REPM
REPM
PC
REF
intACT
intPM
intPC
intRE
intWE
intPM1
RA[12:0]
RAa
RAb
RAc
RAc
QAa
CA[3:0]
CAa
CAb
CAc
CAd

FIG.15

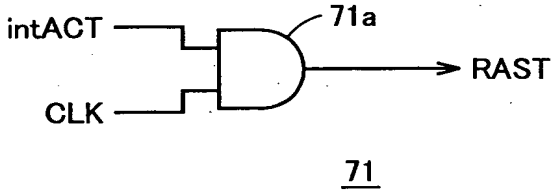


FIG.16

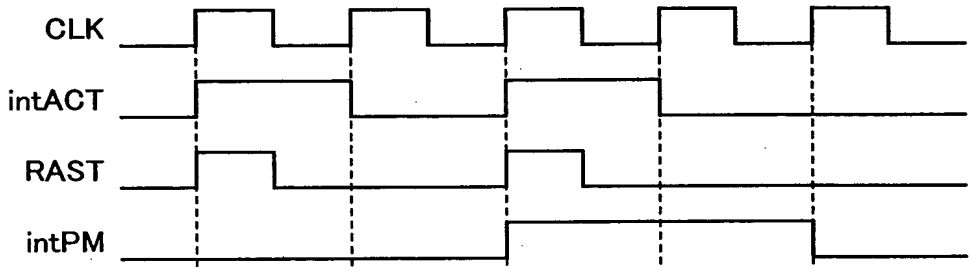


FIG.17

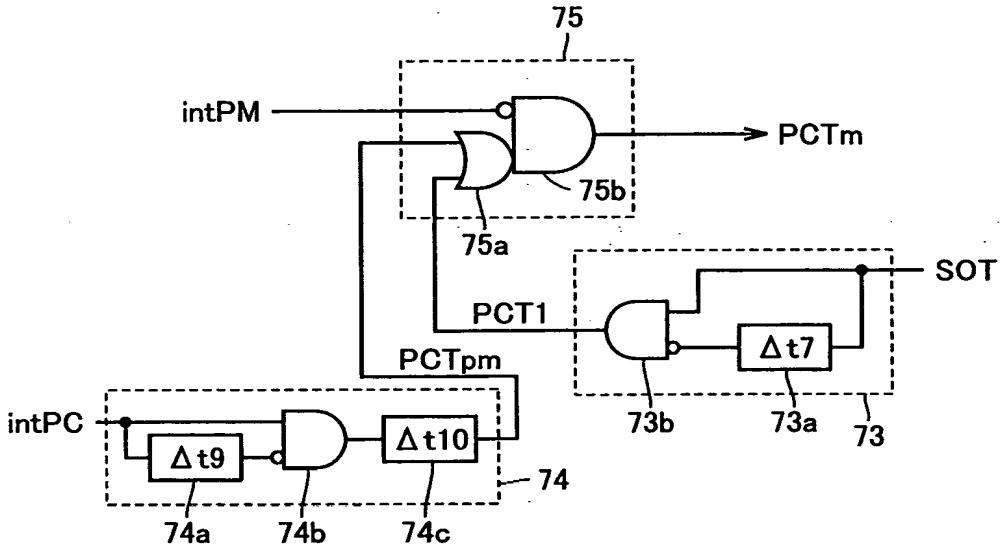


FIG.18

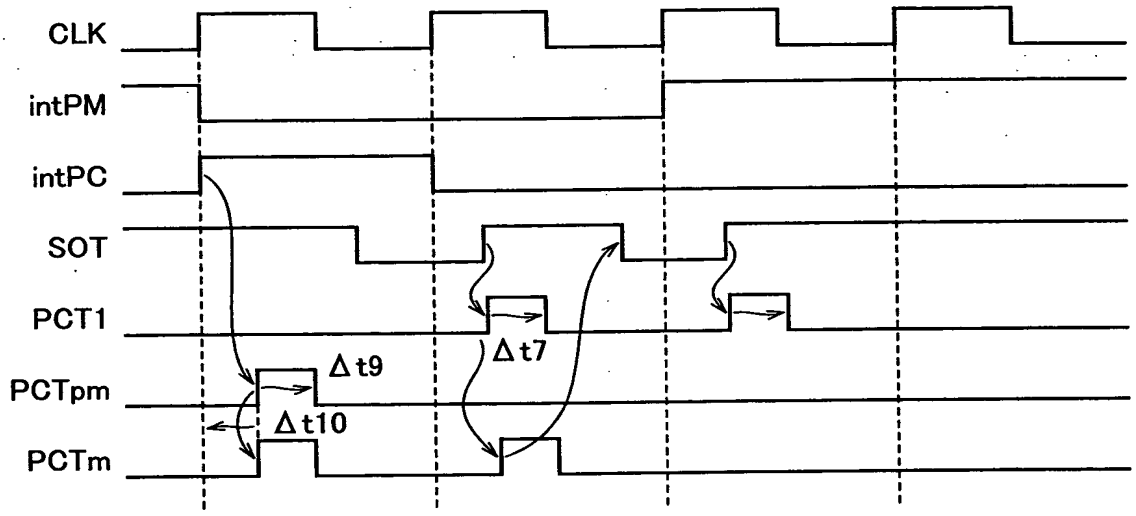


FIG.19

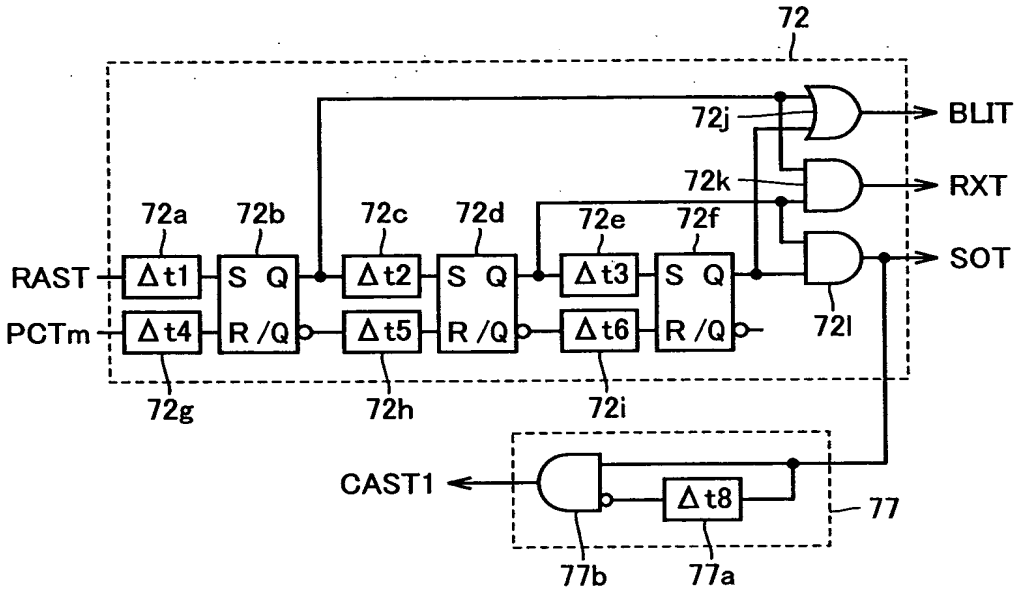

72
72j
BLIT
72k
RXT
SOT
72a
72b
72c
72d
72e
72f
RAST
Δt1
S Q
Δt2
S Q
Δt3
S Q
PCTm
Δt4
R /Q
Δt5
R /Q
Δt6
R /Q
72l
72g
72h
72i
CAST1
Δt8
77
77b
77a

FIG.20

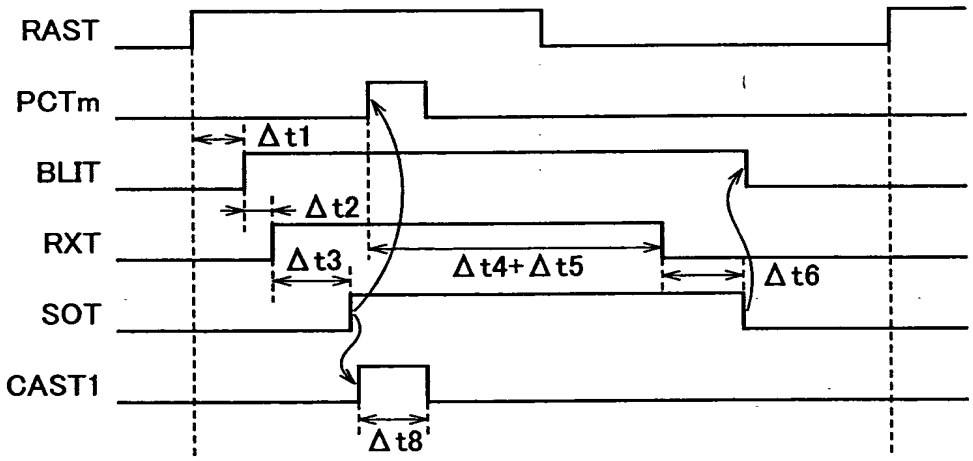

RAST
PCTm
Δt1
BLIT
Δt2
RXT
Δt3
Δt4+Δt5
Δt6
SOT
CAST1
Δt8

FIG.21

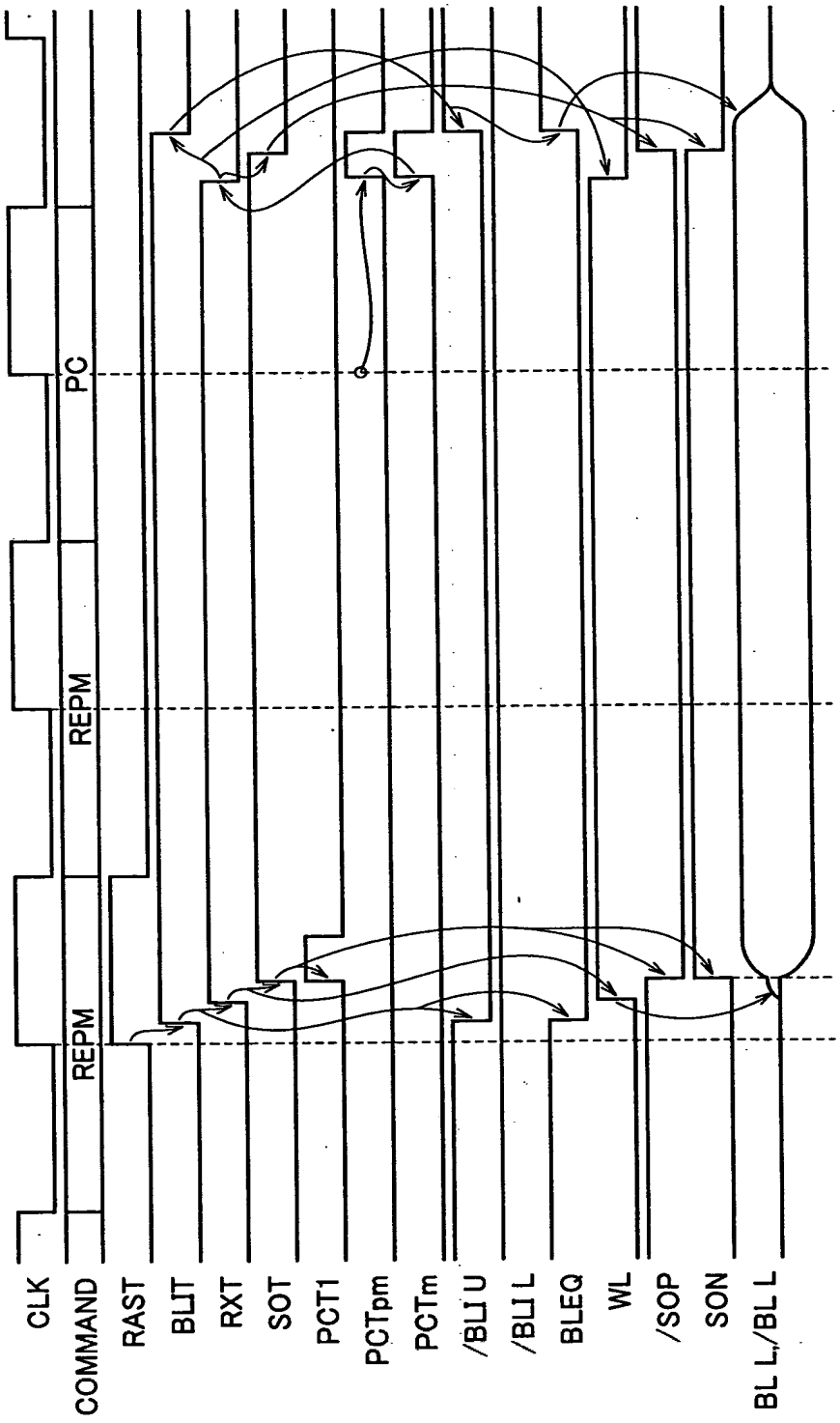

CLK
COMMAND
RAST
BLIT
RXT
SOT
PCT1
PCTpm
PCTm
/BLI U
/BLI L
BLEQ
WL
/SOP
SON
BL L,/BL L
PC
REPM
REPM

FIG.22

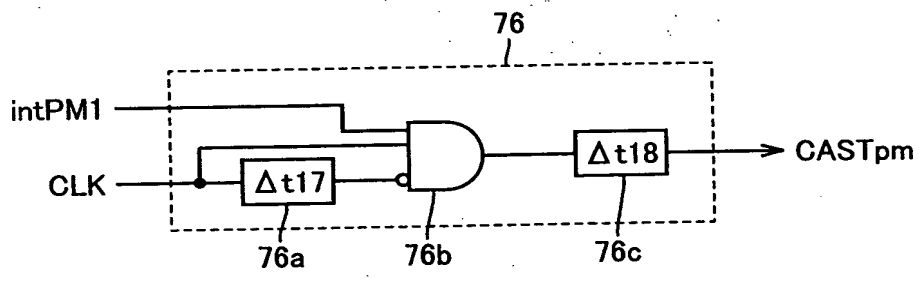

76
intPM1
CLK
Δt17
Δt18
CASTpm
76a
76b
76c

FIG.23

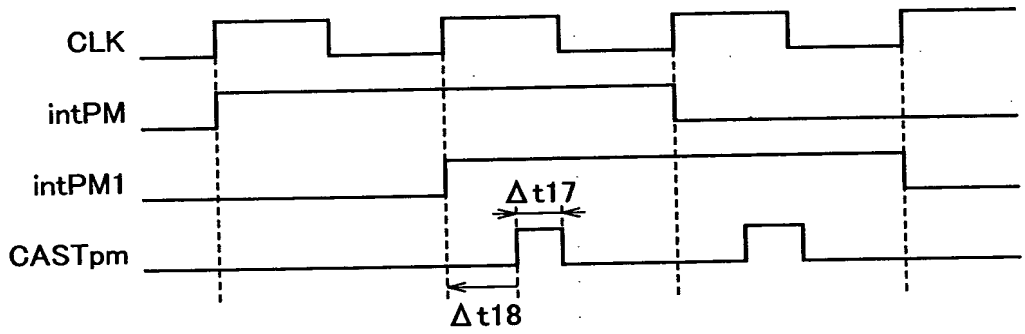

CLK
intPM
intPM1
CASTpm
Δt17
Δt18

FIG.24

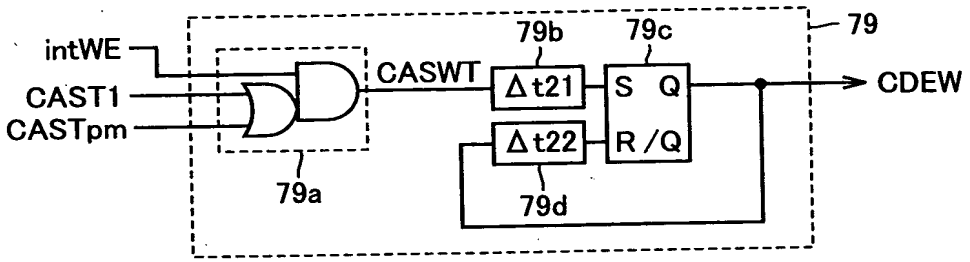

intWE
CAST1
CASTpm
79a
CASWT
79b
Δt21
79c
S Q
R /Q
Δt22
79d
79
CDEW

FIG.25

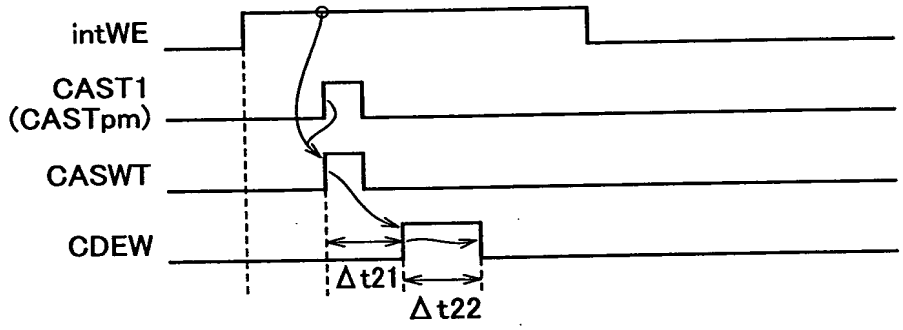

intWE
CAST1
(CASTpm)
CASWT
CDEW
Δt21
Δt22

FIG.26A

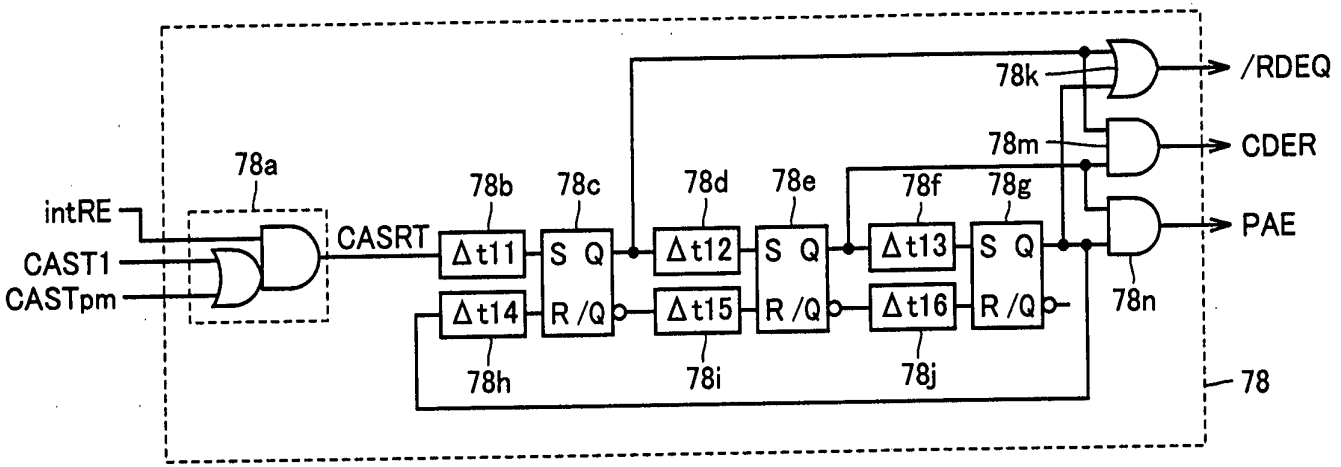


FIG.26B

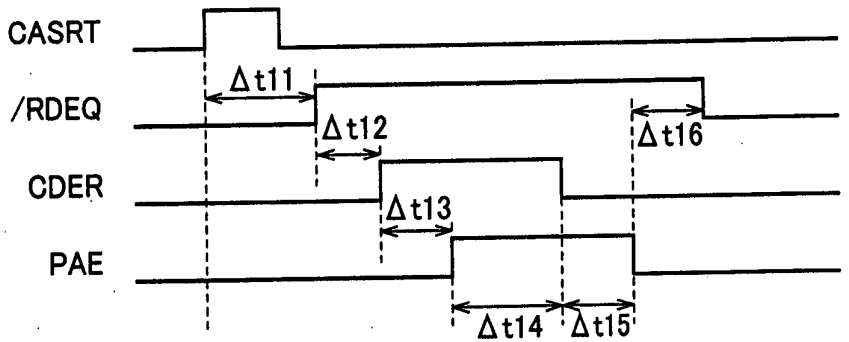


FIG.27

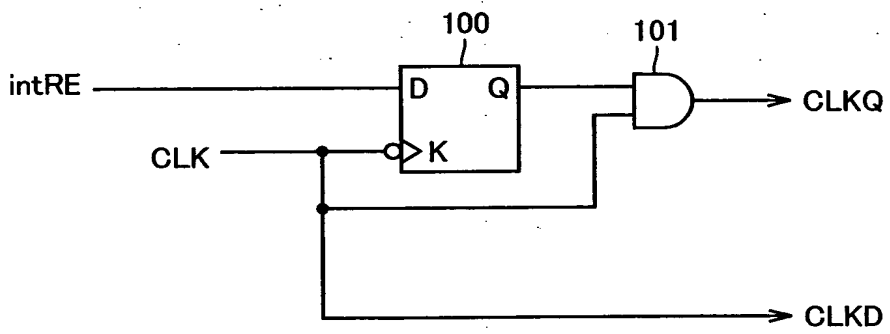

100
101
intRE
D
Q
CLKQ
CLK
K
CLKD

FIG.28

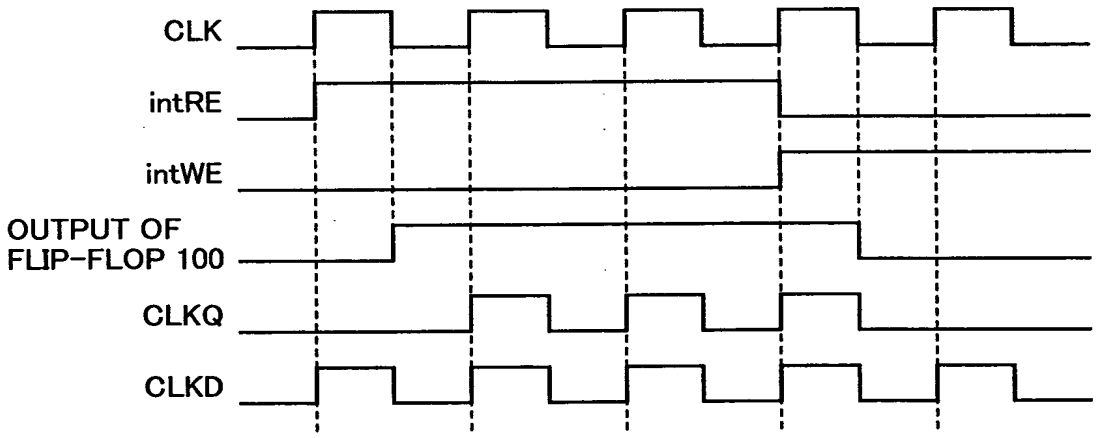

CLK
intRE
intWE
OUTPUT OF
FLIP-FLOP 100
CLKQ
CLKD

FIG.29

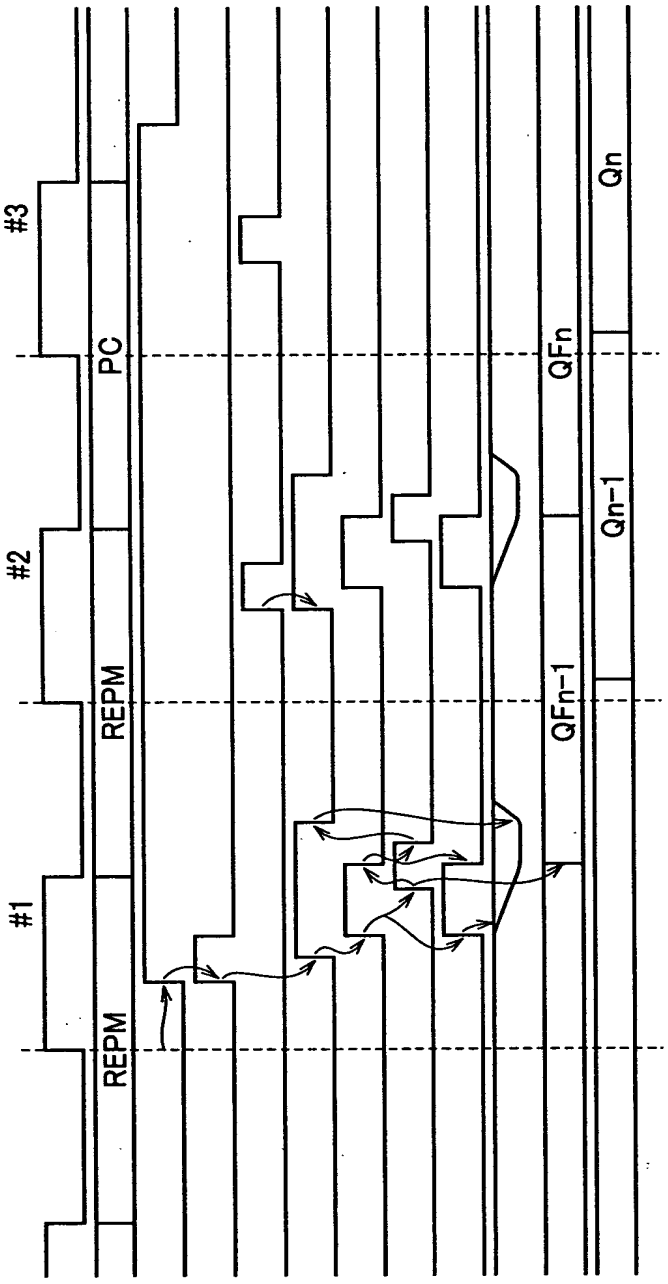

#1
#2
#3
REPM
REPM
PC
CLK
COMMAND
SOT
CAST1
CASTpm
/RDEQ
CDER
PAE
CSLR
RD,/RD
QF[127:0]
Q[127:0]
QFn-1
QFn
Qn-1
Qn

FIG.30

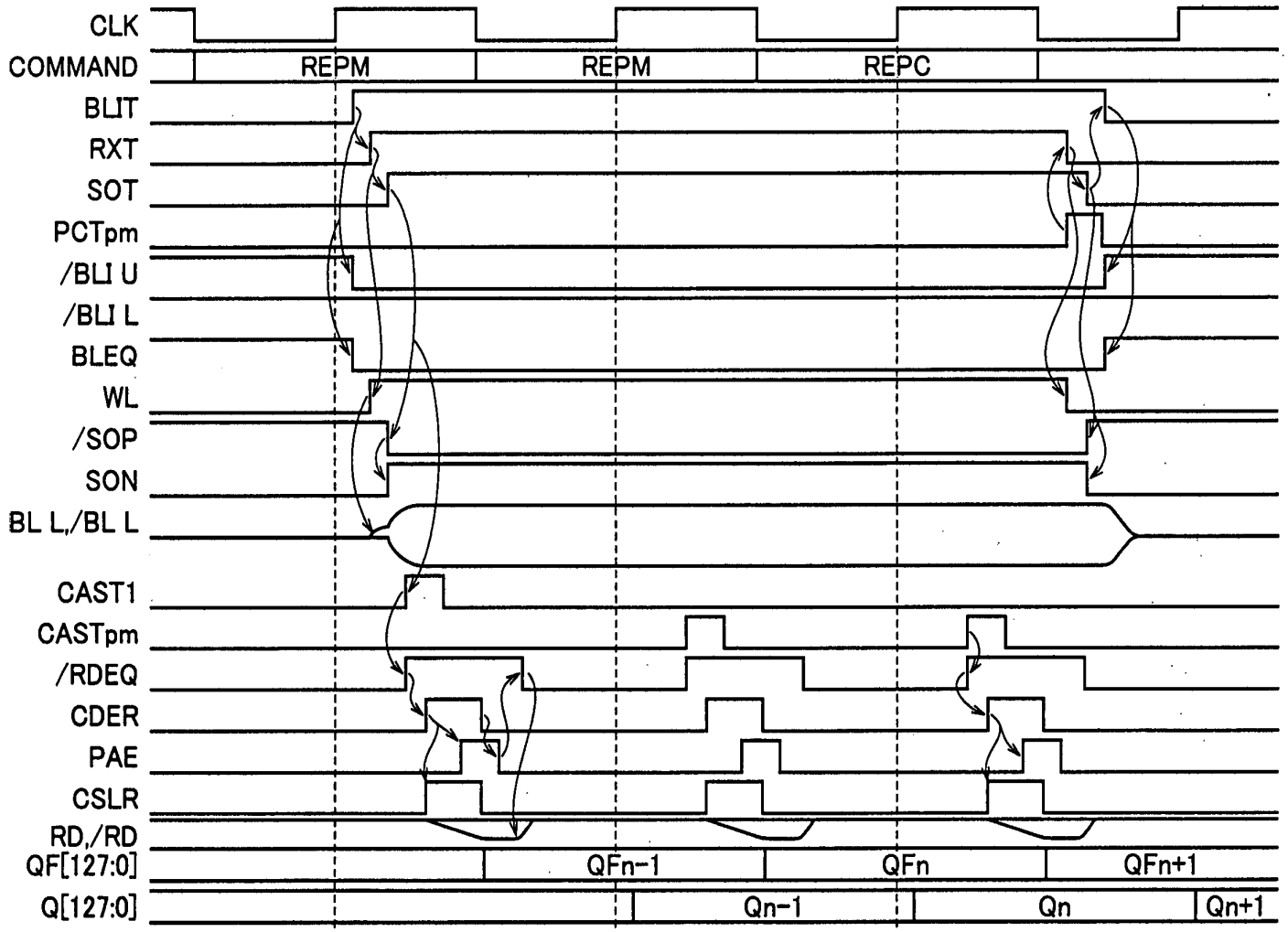

CLK
COMMAND
REPM
REPM
REPC
BLIT
RXT
SOT
PCTpm
/BLI U
/BLI L
BLEQ
WL
/SOP
SON
BL L,/BL L
CAST1
CASTpm
/RDEQ
CDER
PAE
CSLR
RD,/RD
QF[127:0]
QFn-1
QFn
QFn+1
Q[127:0]
Qn-1
Qn
Qn+1

FIG.31

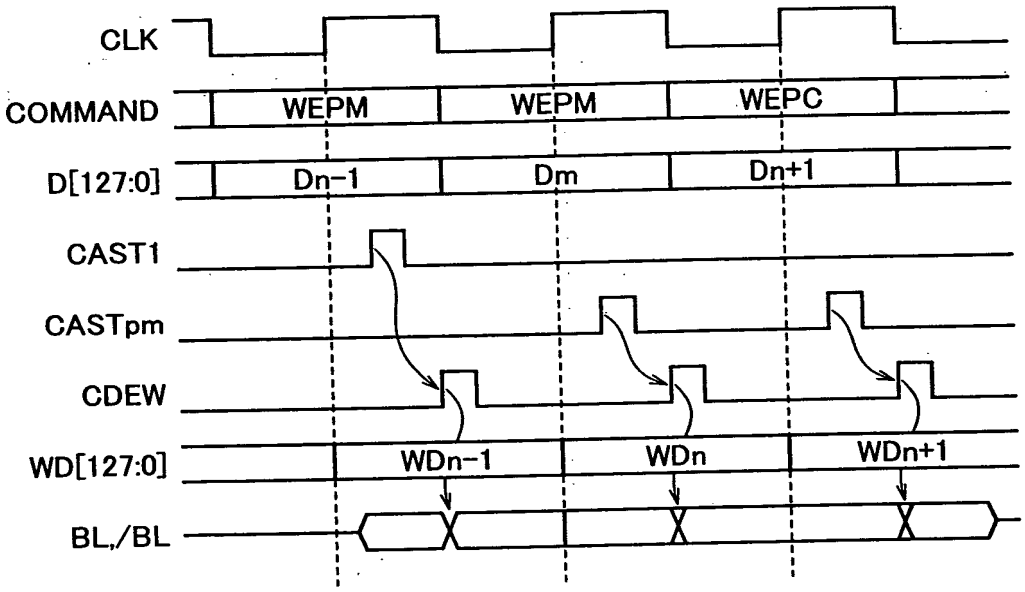


FIG.32

MNEMONIC	RE	WE	REF	PM	PC	FUNCTION
MRS	H	H	H	H	H	MODE REGISTER SET

FIG.33

	A[16:1]	A[0]
WITHOUT PAGE FUNCTION	DON'T CARE	L
WITH PAGE FUNCTION	DON'T CARE	H

FIG.34

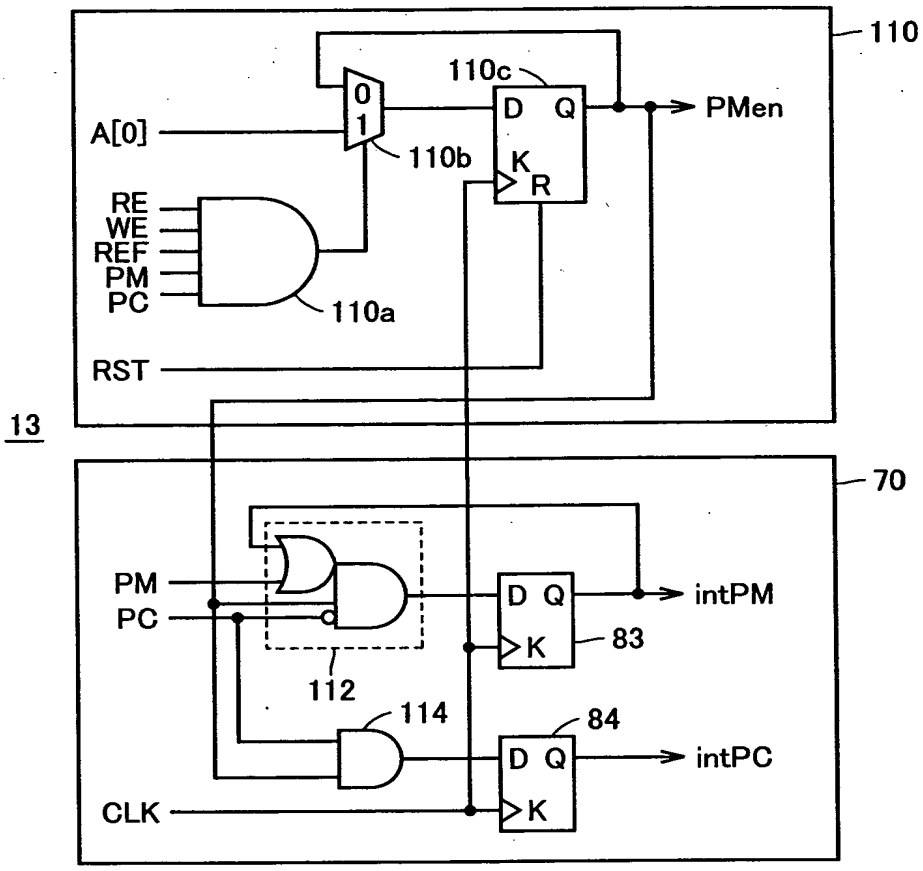

110
110c
D Q
PMen
A[0]
0
1
110b
K
R
RE
WE
REF
PM
PC
110a
RST
13
70
PM
PC
D Q
intPM
K
83
112
114
84
D Q
intPC
CLK
K

FIG.35

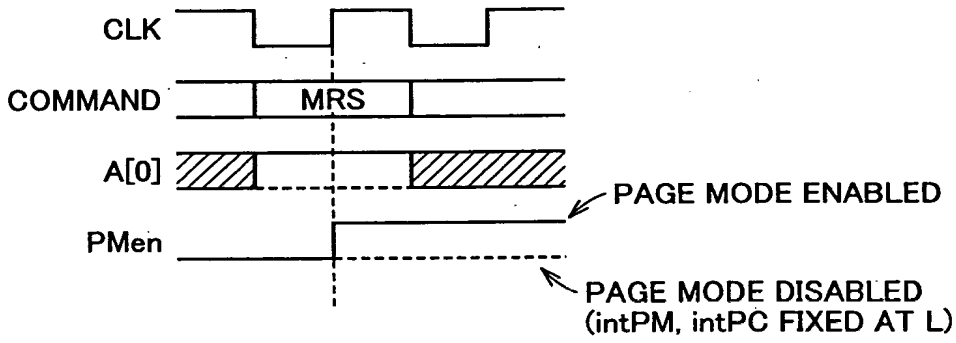

CLK
COMMAND
MRS
A[0]
PAGE MODE ENABLED
PMen
PAGE MODE DISABLED
(intPM, intPC FIXED AT L)

FIG.36

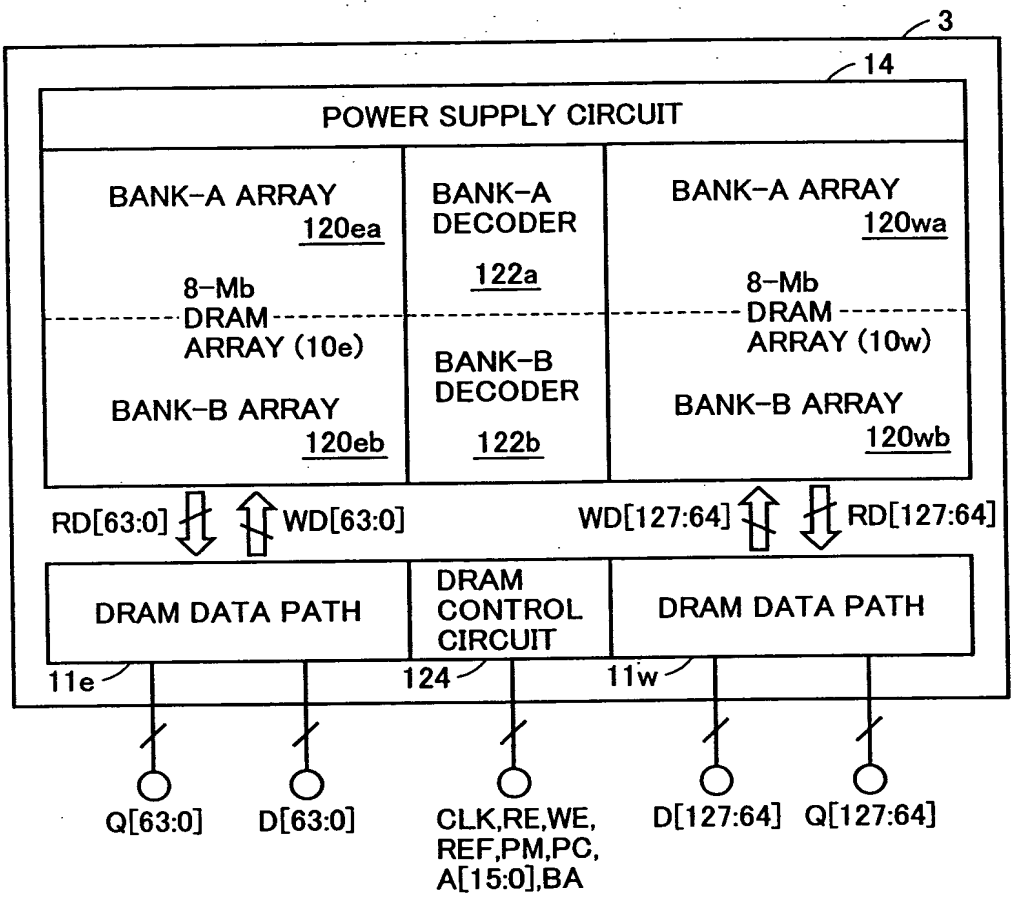

3
14
POWER SUPPLY CIRCUIT
BANK-A ARRAY
120ea
8-Mb
DRAM
ARRAY (10e)
BANK-B ARRAY
120eb
BANK-A
DECODER
122a
BANK-B
DECODER
122b
BANK-A ARRAY
120wa
8-Mb
DRAM
ARRAY (10w)
BANK-B ARRAY
120wb
RD[63:0]
WD[63:0]
WD[127:64]
RD[127:64]
DRAM DATA PATH
DRAM
CONTROL
CIRCUIT
DRAM DATA PATH
11e
124
11w
Q[63:0]
D[63:0]
CLK,RE,WE,
REF,PM,PC,
A[15:0],BA
D[127:64]
Q[127:64]

FIG.37

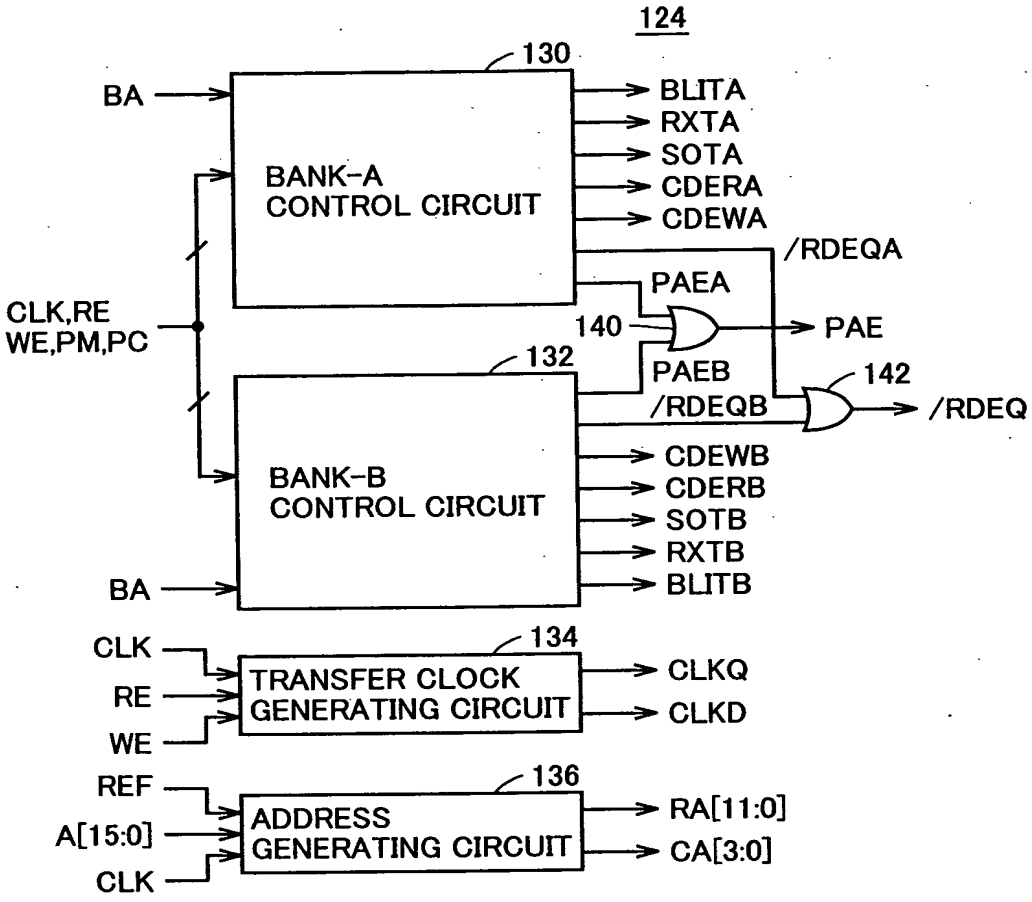

124
130
BA
BANK-A
CONTROL CIRCUIT
BLITA
RXTA
SOTA
CDERA
CDEWA
/RDEQA
PAEA
CLK,RE
WE,PM,PC
140
PAE
132
PAEB
142
/RDEQB
/RDEQ
BANK-B
CONTROL CIRCUIT
CDEWB
CDERB
SOTB
RXTB
BLITB
BA
CLK
RE
WE
134
TRANSFER CLOCK
GENERATING CIRCUIT
CLKQ
CLKD
REF
A[15:0]
CLK
136
ADDRESS
GENERATING CIRCUIT
RA[11:0]
CA[3:0]

FIG.38

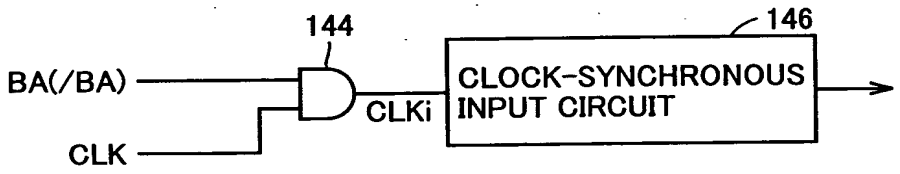

144
146
BA(/BA)
CLK
CLKi
CLOCK-SYNCHRONOUS
INPUT CIRCUIT

FIG.39

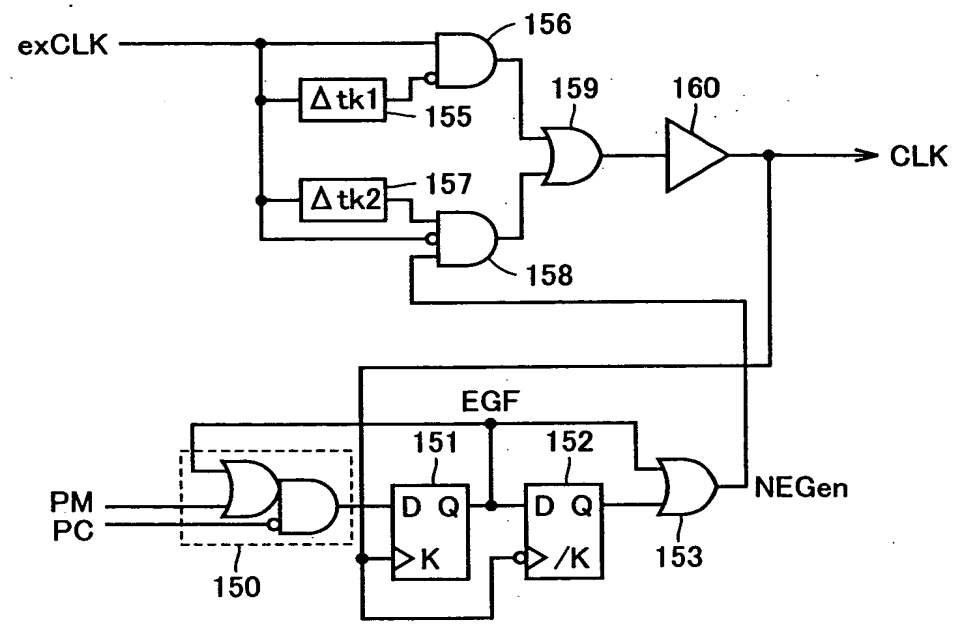

exCLK
156
Δtk1
155
159
160
CLK
Δtk2
157
158
EGF
151
152
PM
PC
D Q
K
D Q
/K
NEGen
153
150

FIG.40

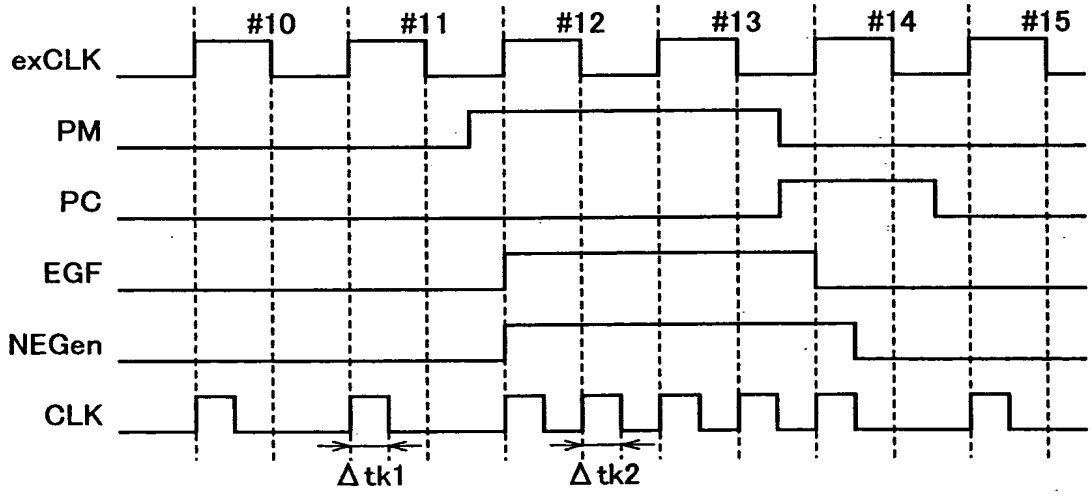

#10
#11
#12
#13
#14
#15
exCLK
PM
PC
EGF
NEGen
CLK
Δtk1
Δtk2

FIG.41

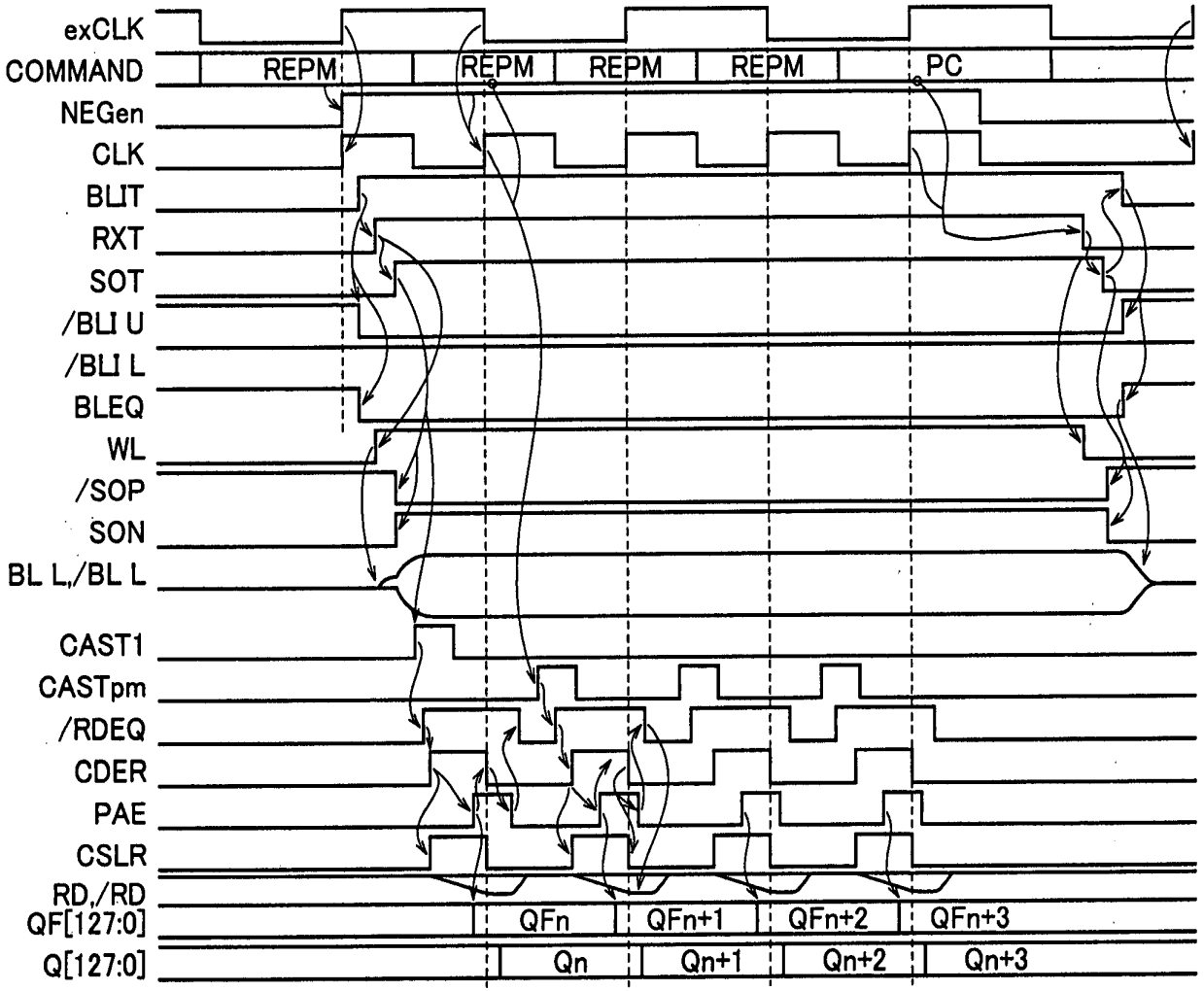

exCLK
COMMAND
REPM
REPM
REPM
REPM
PC
NEGen
CLK
BLIT
RXT
SOT
/BLI U
/BLI L
BLEQ
WL
/SOP
SON
BL L,/BL L
CAST1
CASTpm
/RDEQ
CDER
PAE
CSLR
RD,/RD
QF[127:0]
QFn
QFn+1
QFn+2
QFn+3
Q[127:0]
Qn
Qn+1
Qn+2
Qn+3

FIG.42

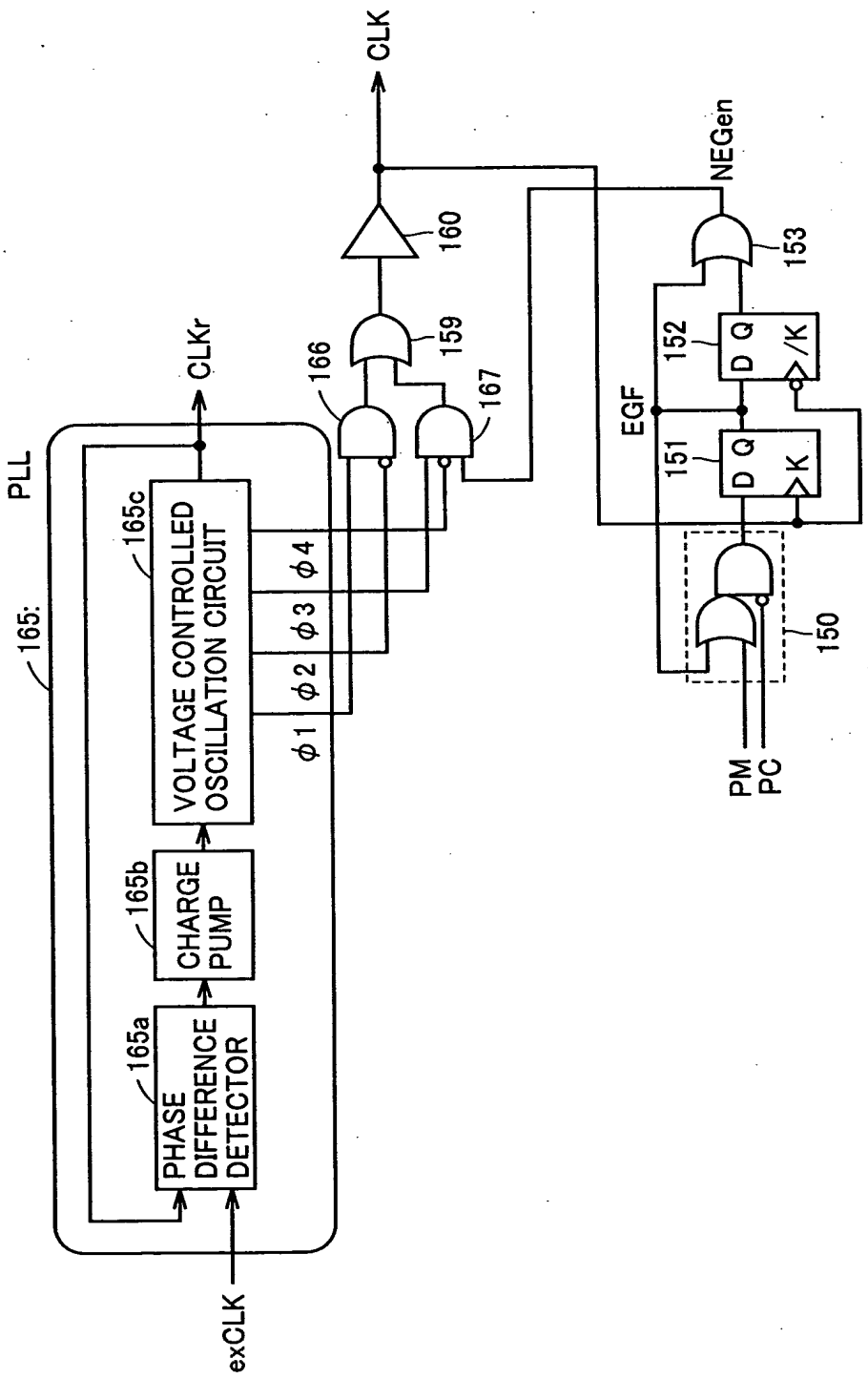

exCLK
PLL
165:
PHASE DIFFERENCE DETECTOR
165a
CHARGE PUMP
165b
VOLTAGE CONTROLLED OSCILLATION CIRCUIT
165c
CLKr
φ1
φ2
φ3
φ4
166
167
159
160
CLK
NEGen
153
152
151
D Q
/K
D Q
K
EGF
150
PM
PC

FIG.43

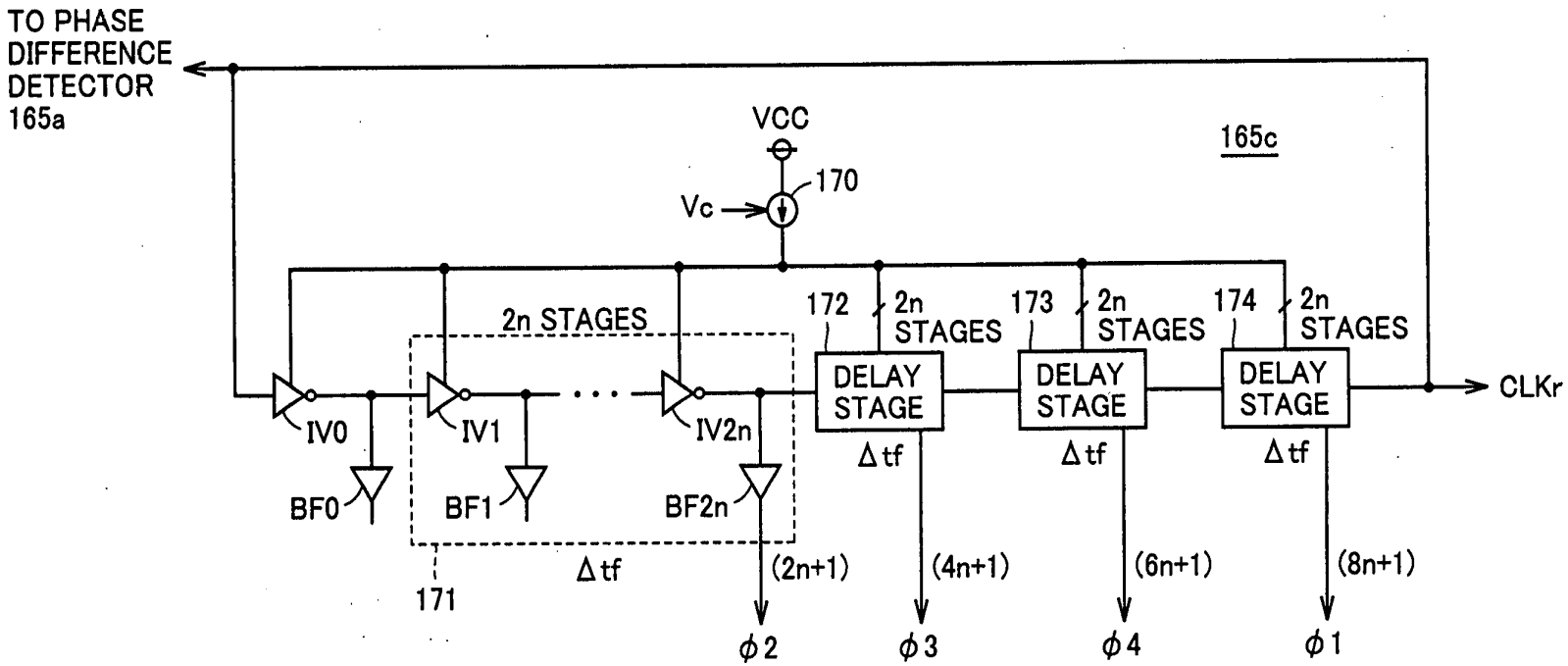

TO PHASE DIFFERENCE DETECTOR 165a
VCC
165c
Vc
170
2n STAGES
172
2n STAGES
173
2n STAGES
174
2n STAGES
DELAY STAGE
DELAY STAGE
DELAY STAGE
CLKr
IV0
IV1
IV2n
BF0
BF1
BF2n
Δtf
Δtf
Δtf
Δtf
171
(2n+1)
(4n+1)
(6n+1)
(8n+1)
φ2
φ3
φ4
φ1

FIG.44

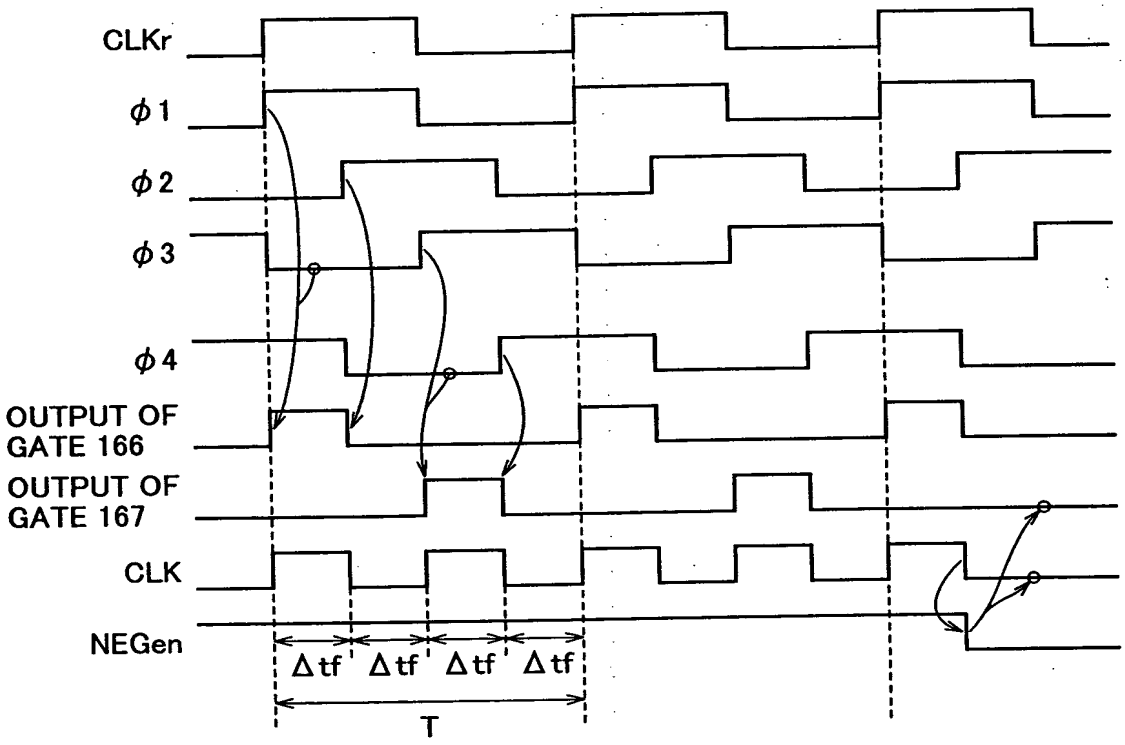
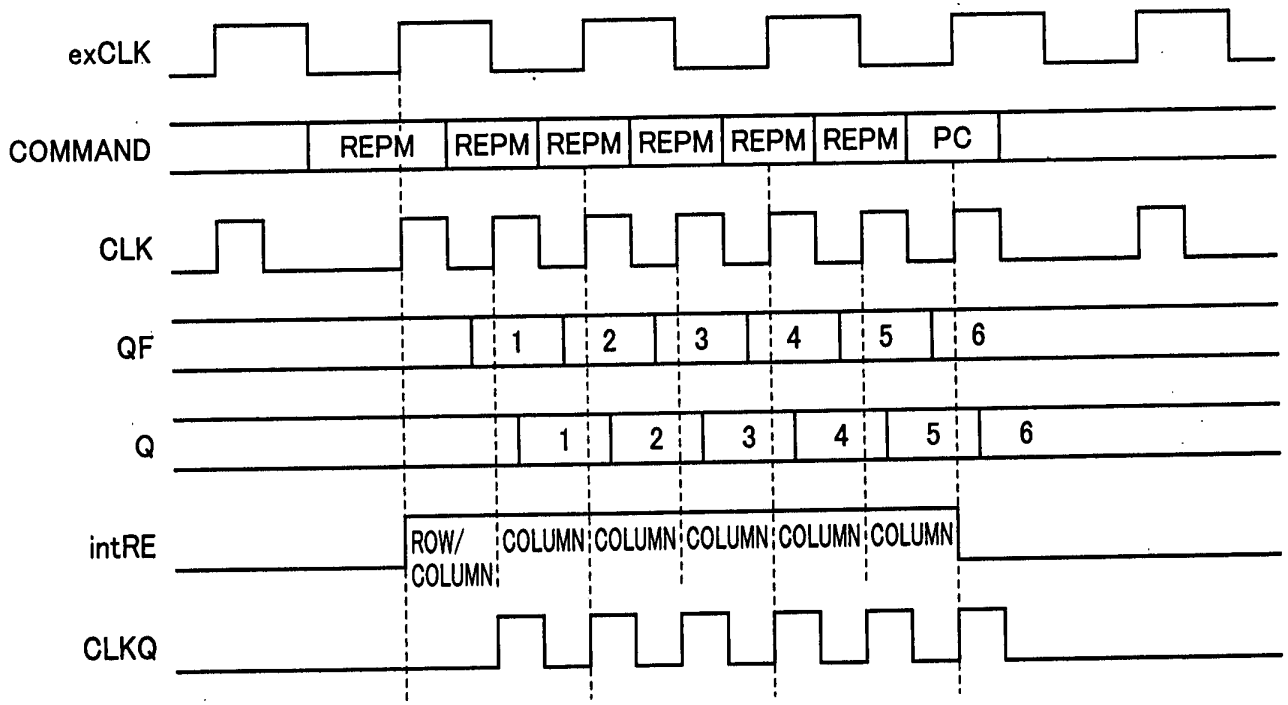

CLKr
φ1
φ2
φ3
φ4
OUTPUT OF GATE 166
OUTPUT OF GATE 167
CLK
NEGen
Δtf
Δtf
Δtf
Δtf
T

FIG.45


exCLK
COMMAND
REPM
REPM
REPM
REPM
REPM
REPM
PC
CLK
QF
1
2
3
4
5
6
Q
1
2
3
4
5
6
intRE
ROW/
COLUMN
COLUMN
COLUMN
COLUMN
COLUMN
COLUMN
CLKQ